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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/529,114	03/16/2006	Kevin Derichs	21561-0014US1	1774

26233 7590 03/09/2009

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EXAMINER	
PATEL, PREMAL R	

ART UNIT	PAPER NUMBER
2629	

NOTIFICATION DATE	DELIVERY MODE
03/09/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATDOCTC@fr.com

Office Action Summary	Application No.	Applicant(s)	
	10/529,114	DERICHS, KEVIN	
	Examiner	Art Unit	
	PREMAL PATEL	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02/25/2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/24/05; 12/1/05; 12/27/05; 11/1/06; 7/17/08; 10/31/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. **Claim 3, 16 and 29** are objected to because of the following informalities: citation of "a low impedance state" on line 4 should be corrected to "said low impedance state"; citation of "a high impedance state" on line 5 should be corrected to "said high impedance state". Appropriate correction is required.

2. **Claim 10, 23 and 36** are objected to because of the following informalities: citation of "a first threshold" on line 8 should be corrected to "said first threshold". Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. **Claim 5, 18 and 31** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claim in lines 1-2 recites "a cycle time for selectively charging and discharging said region of overlap is sufficiently short" and lines 3-4 recites "said cycle time for selectively charging and discharging said region of overlap is sufficiently long". Both the limitations are contradicting each other, therefore the claim is rendered as indefinite.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 1, 2, 4, 5, 9, 14, 15, 17, 18 and 22** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kajihara et al. (6,677,923) in view of Nakano et al. (2002/0158859).

Regarding **claims 1 and 14**, Kajihara teaches a display, comprising: a first set conductive control lines (1004; **Fig 10**); a second set of conductive control lines (1005; **Fig 10**); a matrix of pixels (A; **Fig 10**) overlapping between said first set of control lines and said second set of conductive control lines (**Fig 10**); a first select mechanism (41; **Fig 6**) coupled to said matrix of pixels, wherein said first select mechanism is configured to selectively apply an in-line impedance (**column 17, lines 27-34**) to a control line of said first set of conductive control lines (**column 17, lines 27-34**); and a second select mechanism (903; **Fig 9**) coupled to said matrix of pixels, wherein said second select mechanism is configured to selectively apply a drive voltage (**Column 2; line 27**) to each conductive line of said second set of conductive lines.

Kajihara fails to teach the control lines being parallel, co-planer, spaced apart control lines; planes of second set of control lines is parallel to plane of first set of control lines

and second set of conductive control lines are perpendicular to control lines of said first set of conductive control lines; as claimed.

Nakano teaches a display device wherein the control lines being parallel (**para [0105]**), co-planer, spaced apart control lines; planes of second set of control lines is parallel to plane of first set of control lines (**Fig 1**) and second set of conductive control lines are perpendicular (**para [0105]**) to control lines of said first set of conductive control lines (**para [0105]**) (**Note: Para [0105]** clearly teaches the gate electrodes and source electrode lines are parallel, it also teaches the source and gate lines are perpendicular to each other and regarding the two planes being parallel is shown in **Fig 1**.)

It would have been obvious to one of ordinary skill in the art at the time of invention to have modified the device of Kajihara with the structure of display device as taught by Nakano, because this will result simplify the structure if the display device and reduce the production cost.

Regarding **claims 2 and 15**, Kajihara further teaches, the display, wherein said first select mechanism is further configured to selectively toggle control lines of said first set of conductive control lines between a low impedance state and a high impedance state (**column 17; lines 37-34**).

Regarding **claims 4 and 17**, Kajihara further teaches, the display, wherein a pixel (a region) of said matrix of pixels between a conductive line (**Fig 10**) of said first set of conductive control lines and a conductive line (**Fig 10**) of said second set of

conductive control lines is selectively charged and discharge (**column 18; lines 4-12**) (Note: Regarding selectively charged and discharged is same as the predetermined time as cited).

Regarding **claims 5 and 18**, Kajihara further teaches, the display, wherein a cycle time (a predetermined time; **column 18, lines 5**) for selectively charging and discharging said pixel of said matrix of pixels is sufficiently short such that an active device will not be deactivated and an inactive device will not be activated, wherein said cycle time for selectively charging and discharging said pixel of said matrix of pixels is sufficiently long such that an active device will discharge to below an activation threshold and an inactive device will charge beyond said activation threshold (**Fig 8; column 18, lines 4-28**) (**Note:** Because the claim languages determines the claim to be indefinite as explained above in 112 2nd para rejection; this claim is interpreted as explained by Fig 8 and column 18, lines 4-28 describing the charging /discharging of active/inactive pixel with respect to different timing).

Regarding **claims 9 and 22**, Kajihara further teaches, the display, wherein said first set of parallel, co-planar conductive control lines and said second set of parallel, co-planar conductive control lines are driven at both ends from a common signal source (905; **Fig 9; column 1, lines 53-56**).

7. **Claims 27, 28, 30, 31 and 35** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kajihara et al. (6,677,923) in view of Nakano et al. (2002/0158859) and Millman et al. (2002/0075251).

Regarding **claim 27**, Kajihara teaches a display, comprising: a first set conductive control lines (1004; **Fig 10**); a second set of conductive control lines (1005; **Fig 10**); a matrix of pixels (A; **Fig 10**) overlapping between said first set of control lines and said second set of conductive control lines (Fig 10); a first select mechanism (41; **Fig 6**) coupled to said matrix of pixels, wherein said first select mechanism is configured to selectively apply an in-line impedance (**column 17, lines 27-34**) to a control line of said first set of conductive control lines (**column 17, lines 27-34**); and a second select mechanism (903; **Fig 9**) coupled to said matrix of pixels, wherein said second select mechanism is configured to selectively apply a drive voltage (**Column 2; line 27**) to each conductive line of said second set of conductive lines.

Kajihara fails to teach the control lines being parallel, co-planer, spaced apart control lines; planes of second set of control lines is parallel to plane of first set of control lines and second set of conductive control lines are perpendicular to control lines of said first set of conductive control lines; as claimed.

Nakano teaches a display device wherein the control lines being parallel (**para [0105]**), co-planer, spaced apart control lines; planes of second set of control lines is parallel to plane of first set of control lines (**Fig 1**) and second set of conductive control lines are perpendicular (**para [0105]**) to control lines of said first set of conductive control lines

(**para [0105]**) (**Note: Para [0105]** clearly teaches the gate electrodes and source electrode lines are parallel, it also teaches the source and gate lines are perpendicular to each other and regarding the two planes being parallel is shown in **Fig 1**.)
It would have been obvious to one of ordinary skill in the art at the time of invention to have modified the device of Kajihara with the structure of display device as taught by Nakano, because this will result simplify the structure if the display device and reduce the production cost.

Kajihara and Nakano fail to teach a processor; a memory unit; an input mechanism; and a bus system for coupling the processor to the memory unit, input mechanism; as claimed.
Millman teaches a system comprising a processor (102; **Fig 1**); a memory unit (104; **Fig 1**); an input mechanism (I/o device, 108; **Fig 1**); and a bus system (106; **Fig 1**) for coupling the processor to the memory unit, input mechanism (**Fig 1**).
It would have been obvious to one of ordinary skill in the art at the time of invention to have the display device of Kajihara and Nakano with the teaching of Millman, because the software routine adjusts video timing signal and conservers power in response to detection.

Regarding **claims 28, 30, 31 and 35**, they are rejected same as claims 2, 4, 5 and 7, as explained above.

8. **Claims 6 and 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kajihara et al. (6,677,923) in view of Nakano et al. (2002/0158859) as applied to claims 1 and 14 above, and further in view of Odake et al. (6,426,595).

Regarding **claims 6 and 19**, Kajihara and Nakano teaches the display wherein control lines in said second set of conductive control lines are collinear, coplanar, as explained above for claims 1 and 14.

Kajihara and Nakano fail to teach equally splitting control lines with sufficient physical separation to ensure electrical isolation between them; as claimed.

Odake teaches a flat display apparatus wherein control lines are split equally into two halves with sufficient physical separation to ensure electrical isolation between them (YA, YB; **Fig 2, Fig 8**).

It would have been obvious to one of ordinary skill in the art at the time of invention to have modified the display device of Kajihara and Nakano with the control line division as taught by Odake, because this will provide a display having improved luminance, contrast and response of display.

9. **Claims 11, 12, 13, 24, 25 and 26** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kajihara et al. (6,677,923) in view of Nakano et al. (2002/0158859) as applied to claims 1 and 14 above, and further in view of Takeda et al. (**JP 09120934 A**).

Regarding **claims 11, 12, 13, 24, 25 and 26** Kajihara and Nakano teaches the display device as explained above for claims 1 and 14 above.

Kajihara and Nakano fails to teach the material of the control lines configured to selectively change its resistance and material comprises doped perovskites; as claimed.

Takeda teaches a conductor line contains perovskite dielectric (**Abstract**) (**Note:** this is the material).

It would have been obvious to one of ordinary skill in the art at the time of invention to have modified the control line of display device as taught by Kajihara and Nakano with the teaching of Takeda, because this would control lines with variable resistance, thus improve the display.

10. **Claim 32** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kajihara et al. (6,677,923) in view of Nakano et al. (2002/0158859) and Millman et al. (2002/0075251) as applied to claim 27 above, and further in view of Odake et al. (6,426,595).

Regarding **claim 32**, Kajihara, Nakano and Millman teaches the display wherein control lines in said second set of conductive control lines are collinear, coplanar, as explained above for claims 27.

Kajihara, Nakano and Millman fail to teach equally splitting control lines with sufficient physical separation to ensure electrical isolation between them; as claimed.

Odake teaches a flat display apparatus wherein control lines are split equally into two halves with sufficient physical separation to ensure electrical isolation between them (YA, YB; **Fig 2, Fig 8**).

It would have been obvious to one of ordinary skill in the art at the time of invention to have modified the display device of Kajihara, Nakano and Millman with the control line division as taught by Odake, because this will provide a display having improved luminance, contrast and response of display.

11. **Claims 37, 38 and 39** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kajihara et al. (6,677,923) in view of Nakano et al. (2002/0158859) and Millman et al. (2002/0075251) as applied to claim 27 above, and further in view of Takeda et al. (**JP 09120934 A**).

Regarding **claims 11, 12, 13, 24, 25 and 26,** Kajihara, Nakano and Millman teaches the display device as explained above for claim 27 above.

Kajihara and Nakano fails to teach the material of the control lines configured to selectively change its resistance and material comprises doped perovskites; as claimed.

Takeda teaches a conductor line contains perovskite dielectric (**Abstract**) (**Note:** this is the material).

It would have been obvious to one of ordinary skill in the art at the time of invention to have modified the control line of display device as taught by Kajihara, Nakano and

Millman with the teaching of Takeda, because this would control lines with variable resistance, thus improve the display.

Allowable Subject Matter

12. **Claims 3, 8, 10, 16, 21, 23, 29, 34 and 36** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

13. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claims 3, 16 and 29, prior art fails to teach, "**The addressing mechanism, wherein said first selected mechanism further comprises: a row select sequencer configured to sequentially activate subsequent control lines in said first set of conductive control lines, wherein a selected control line in said first set of conductive control lines is placed in a low impedance state while non-selected control lines in said first set of conductive control lines are placed in a high impedance state; a clock mechanism configured to determine a duration of time said selected control line is in said low impedance state; and a synchronizing mechanism configured to synchronize loading and encoding of data to said clocking mechanism and said selected control line such that said data is loaded and processed during said duration of time said selected control line is in said low impedance state**".

Regarding claims 8, 21 and 34, prior art fails to teach, "**The addressing mechanism, wherein said polarity of said field is reversed in said cyclic manner by driving a pair of comparators from a voltage divider and oscillating a control logic signal distributed across appropriate reference potentials of opposing polarity**".

Regarding claims 10, 23 and 36, prior art fails to teach, "**The addressing mechanism, wherein a first set of voltage levels are applied to said first set of parallel, co-planar conductive control lines, wherein a second set of voltage levels are applied to said second set of parallel, co-planar conductive control lines, wherein an activated device at a region of overlap between a conductive line of said first set of conductive control lines and a conductive line of said second set of conductive control lines is deactivated when a difference between one of said second set of voltage levels and one of said first set of voltage levels is below a first threshold, wherein an activated device at said region of overlap is deactivated when a difference between one of said second set of voltage levels and one of said first set of voltage levels is less than a first threshold, wherein a deactivated device at said region of overlap is activated when a difference between one of said second set of voltage levels and one of said first set of voltage levels exceeds a second threshold.**"

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PREMAL PATEL whose telephone number is (571)270-5892. The examiner can normally be reached on Monday to Friday, 6:30 to 4:00, with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on (571)272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/P. P./
Examiner, Art Unit 2629

/Amare Mengistu/

Supervisory Patent Examiner, Art Unit 2629